

#### LAKIREDDY BALI REDDY COLLEGE OF ENGINEERING

(AUTONOMOUS

Accredited by NAAC & NBA (CSE, IT, ECE, EEE & ME)

Approved by AICTE, New Delhi and Affiliated to JNTUK, Kakinada

L.B.Reddy Nagar, Mylavaram-521230, Krishna Dist, Andhra Pradesh, India



#### ANALOG INTEGRATED CIRCUITS

#### **UNIT-I**

- > INTRODUCTION
- > TRANSISTOR CURRENT SOURCE
- DIFFERENTIAL AMPLIFIERS

#### **Contents**

- 1. IC Definition and Types
- 2. IC Features and Difference b/w AIC & DIC
- 3. Basic Current Source
- 4. Widlar Current Source
- 5. Cascode Current Source
- 6. Wilson Current Source
- 7. Classifications of Differential Amplifiers and AC-DC analysis
- 8. Dual input Balanced output Differential Amplifiers
- 9. Dual input Unbalanced output Differential Amplifiers
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- 11. Single input Unbalanced output Differential Amplifiers
- 12. Specifications of Differential Amplifiers
- 13. DC Coupling and Cascaded Differential Amplifiers
- 14. Level Translator

### Integrated Circuits:

The term IC means integrated circuit where all the

active of Passive components are fabricated on the same chip. IC is a microscopic ownay of electronic circuits and components that one diffused (or) implanted Advantages: on to the surface of single coystal (or) chip of semiconducting material

- 1 Small Size
- 2. low cost
- 3. Less weight
- a. Fast speed

- 5. low supply voltages
- 6. low power consumption
- 7. Highly reliable
- 8. matched devices.

#### classifications:

-> Based on function ICs are classified into two types. Those are i) Digital Ic ii) Linean IC.

### i) Digital Ic:

- \* These are complete functioning of logic network, such as Grutes, Counters, multiplexers. Demultiplexers and Shift registers.
- \* It is a complete predesigned package, and it requires a power-Supply, 1/p & olp
- \* Digital circuits are primarily concerned with only two Levels of voltage (8) carrent: HIGH (8) LOW
- \* These are easy to design of produced in large quantities as a low cost devices. ii) Linear IC ?
- \* These are equivalents of discrete transistor network, such as Amplifiers, filters, beguency multipliers and modulators.
- \* It requires additional external components for Satisfactory operation.
- Ex External resistors are necessary to control the voltage gain and frequency responce of an op-Amp.

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> Based on fabrication ICS are classified into three types. Those are
                                    -> Bipolan ICS
         i) monolithic Ics
                                    Ly Unipolan Ics
         ii) Thick& Thin film ICS
         iii) Hybrid ICS
 Based on number of components used Ics we clussified into following
   types. Those our
                                               less than 100 -> 1960-1965
        i) Small scale Integration (SSI)
                                               100-1000 -> 1965-1970
                                  (MSI)
                                               1000 - 1,00,000 > 1970-1980
      ii) medium 11
                                  (LSI)
      iii) wage "
                                                more than 1,00,000, 1980-1990
                                  (ULSI)
      iv) Very longe "
                                                move than 1 million, 1990-2000
                                  (ULSI)
       V) Ultra wrige "
                                                 106-107
                                                 717
                                  (CISI)
       vi) traint
```

- → A current mirror is a circuit whose output current is a replicor of the current sent at its input terminal.
- -> A constant current source is an electronic circuit that supplies a constant current to the wad i.e. independent of the voltage across the wad.
- → The constant current sources are widely used in analog integrated circuits as biasing elements and load devices for amplifier stayes.

#### Basic Current Source:

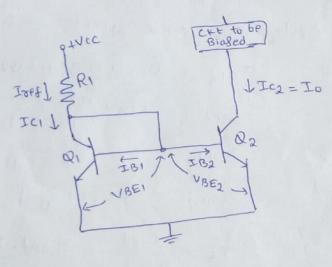
iscuit, the transistors Q14Q2

are matched and the bases

and emitter of Q14Q2 are

tied together and thus have

the same VBE



- The transistor Q1 is connected as a diode by shorting its collector to base, The 1/P current I ref flows through diode-connected transistor Q1 and thus establishes a voltage across Q1. This voltage inturn appears b/w the base femilter of Q2.
  - Thus, as long as \$\text{Q2} is maintained in the active stegion, its collector current Ic2 (Io) will be approximately equal to Iref. Hence the circuit is often referred to as a current mirror
  - This missor effect is however valid only for larger values of B.

from ex (3): for \$>>1 then B = 1 (: Io = Ic = Iref)

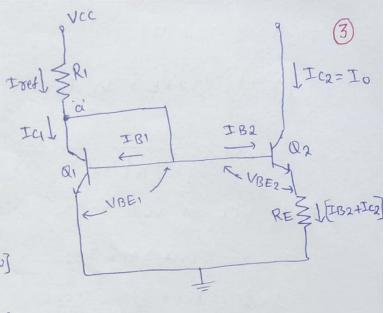
-> Typically To Varied by 31/2 for 50 < B < 200.

(2) (67) the custent mistor circult is to provide a 1.0 mA current with Vcc = 10 V. Affume B=125 and UBE = 0.7 V. Determine (a) the value of RI (b) the value of RI for Ic = 10 MA Sol Criven data Ic = 1 mA Ic = B Iret => Ic = B [Vcc - VBE] (ci)  $R_1 = \frac{\beta}{\beta+2} \left( \frac{V(c-VBE)}{Tc} \right) = \frac{125}{125+2} \left[ \frac{10V-0.7V}{1.mA} \right]$ | R1 = 9.15 KM (b)  $Ic = 10 \mu A$  R1 = B VCC - VBE = 125 + 2 [10V - 0.7V]R1 = 915 KV

### Midlar Current Source:

→ The basic current Source has

a limitation. Whenever, we need low value current source the value of resistance Ri is high [Ex. 2.10 page 67 Roy. chow] and cannot be fabricated economically in IC circuits.



- Therefore, there is a new current source (so) modified current source, which is used to generate a lower current source.
  - -> The circuit differ from the basic current source is only in the emitter resistance RE. Due to RE, VBEZ is less than VBE, and Io is smaller than ICI.

#### Analysis:

Equate eq (i) 
$$\phi$$
 (ii)

$$\begin{bmatrix} \frac{1}{B} + 1 \end{bmatrix} \text{ Ica } RE = VT \text{ In } \left( \frac{TCI}{TC_2} \right)$$

$$RE = \frac{VT}{(1 + \frac{1}{B})} \frac{1}{TC_2} \frac{1}{A} \left( \frac{TCI}{TC_2} \right)$$

$$\rightarrow \text{ Apply kel at node a'}$$

$$Ivef = Ici + Isi + Isa$$

$$Ivef = Ici + \frac{Ici}{B} + \frac{Ica}{B}$$

$$Ivef = Ici \left[ 1 + \frac{1}{B} \right] + \frac{Ica}{B}$$

$$\rightarrow \text{ In widlow current Source } Ica < CICI, \text{ therefore } \frac{Ica}{B} \text{ is } \text{ neglected in } eq \text{ (iii)}.$$

$$\text{Innual } Ivef \cong Ici \left( 1 + \frac{1}{B} \right) \cong Ici \left( \frac{1+B}{B} \right)$$

$$\therefore Ici = \left( \frac{B}{1+B} \right) Ivef$$

$$\rightarrow \text{ (iv)}$$

$$INhere Ivef = Vcc - VBE$$

→ for B>>1 tuen Ic1 = Iref

(3-A)

Design a Widlar current Source for generating of constant current Io = 10 MA. Affume Vcc = 10V, VBE = 0.7V, B = 125. Use VT = 25 mV.

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For widlar current source, we must first decide a Suitable value for Iref. If we choose Iref = ImA, then

$$R_1 = \frac{Vcc - VBE}{Ived} = \frac{10V - 0.7V}{ImA} = \frac{9.3 \times SL}{1}$$

$$PE = \frac{VT}{\left[1 + \frac{1}{\beta}\right] TC2} \ln \left(\frac{TC1}{TC2}\right) = \frac{0.025}{\left(1 + \frac{1}{125}\right) 10 \mu A} \ln \left(\frac{1mA}{10 \mu A}\right)$$

Therefore, the widler current source allows the generation of small currents using small resistors.

### Improved current fource circuits:



- -> A good cuttent Source must meet two requirements.
  - (9) The ofp current Io, should not dependent upon B.
  - (ii) The old resistance of the current source should be very high.
- (a) A current Source with Grain:
- The circuit shown in figure includes a transistor Qz, whose emitter current supplies the base currents of Q1 f Q2.
- -> Apply KCL at node a.

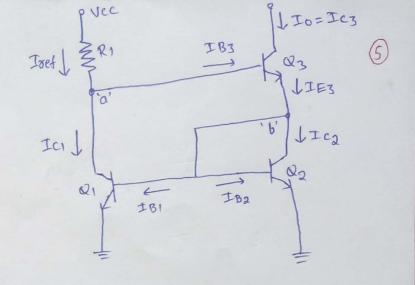
Tref = 
$$Tc_1 + TB_3$$
 $Tref = Tc_1 + TE_3$ 
 $Tref = Tc_1 + Te_2$ 
 $Tref = Tc_1 + Te_3$ 
 $Tref = Tc_1 + Te_3$ 

independent of the B.

 $\rightarrow (1)$ 

# Wilson Current Source:

-> This current source provides an o/p current Io, which is very nearly equal to I ref and also exhibits a Very high of resistance.



-> Apply KCL at node b

$$IE3 = IC2 + IB1 + IB2 = IC2 + 2IB = IC2 + 2IC2 = IC2 \left[1 + \frac{2}{B}\right]$$

$$\longrightarrow (1)$$

- We know mut from fig

IE3 = Ic3+IB3 = Ic3 
$$=$$
 Ic3  $=$  Ic4  $=$  Ic3  $=$  Ic3  $=$  Ic3  $=$  Ic3  $=$  Ic3

$$Ic3\left(1+\frac{1}{\beta}\right) = Ic2\left(1+\frac{2}{\beta}\right)$$

$$Ic3\left(\frac{1+\beta}{\beta}\right) = Ic2\left(\frac{2+\beta}{\beta}\right)$$

$$Ic3\left(\frac{1+\beta}{\beta}\right) = Ic2\left(\frac{2+\beta}{\beta}\right)$$

$$Ic3 = Io = \left(\frac{2+\beta}{1+\beta}\right)Ic2$$

$$\therefore I_0 = \left(\frac{2+\beta}{1+\beta}\right) I_{c_1}$$

-> Apply KCL at node a

Tref = 
$$Ici+IB3$$
 =  $\left(\frac{1+\beta}{2+\beta}\right)Io + \frac{Io}{\beta} = Io\left(\frac{\beta+\beta^2+2+\beta}{\beta(2+\beta)}\right)$ 

$$I_{\delta e4} = I_{\delta} \left[ \frac{\beta^2 + 2\beta + 2}{\beta^2 + 2\beta} \right]$$

$$: To = \left[\frac{\beta^2 + 2\beta}{\beta^2 + 2\beta + 2}\right] Treat$$

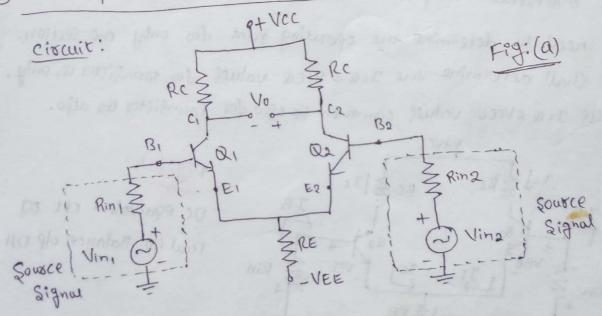
$$: To = \left[\frac{\beta^2 + 2\beta}{\beta^2 + 2\beta + 2}\right] Tret$$
 where  $Tref = \frac{Vcc - 2VBE}{R_1}$ 

# Configurations of Differential Amplifier:

- -> There are four configurations, those are
  - i) Dual PP, Balanced of differential amplifier
  - ii) nual ilp, unbalanced olp "
  - iii) Single ilp, balanced olp "
  - iv) fingle ilp un balance olp "
- -> If old is taken blu the two collectors it is called balanced off
- If the old is taken blw one collector with respect to ground it is called unbalanced old as Single ended old.
- -> If the signal is given to both the ilp terminals it is called dual ilp.
  - -) It the Signal is given to only one i'll terminal and other terminal is grounded it is called single i'lp (8) single ended i'lp.

- Parlameters for a number of reasons.
  - \* The A.c. analysis of differential amplifiers with y- parameters is Simpley, more stright forward, and less cumbersome.
  - The performance equations obtained are easy to remember since mey are not as complex (8) as lengthy as h-parameter equations

# O Dual P/P, Balanced of Differential Amplified:



- -> The two ip Signals Vini & Vina we applied to the bases
  Bi & Ba & transistors Qi & Qa.
- -) the old vo is measured blu the two collectors, cit co which are at the same de potential.
- -> Because of the equal de potential at the two collectors with respect to ground, the olp is referred to es a balance ofp.

### DC Analysis:

- -> To eletermine the operating point values (Ica 4 VCEQ) for the differential amplifier we need to obtain a de equivalent circuit.
- -> The de equivalent circuit can be obtained simply by reducing the ilp Signals Vin 1 d Vina to Zero. The circuit shown in below fig.
- -> The internal resistances of of the ilp Signals one denoted by Rin because Ring = Ring. Since both emitter-biased sections of the differential amplifier are symmetrical.
  - \* We need to determine the operating point for only one section. We shall determine the Ica& VCEQ values for toansistor Q, only. These Ica & VCEQ values can then be used for to angistor as also.

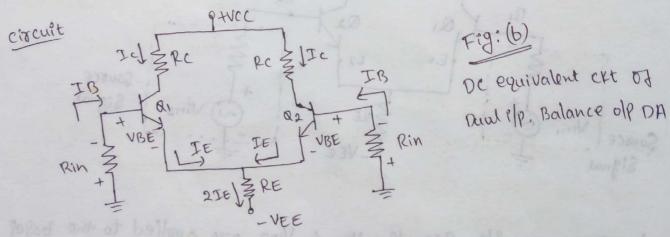


Fig: (b)

-> Apply KVI to the Base-emitter loop of the transistor Q1.

But we know 
$$B = \frac{IC}{IB} \Rightarrow IB = \frac{IC}{B} \Rightarrow IB = \frac{IE}{B}$$
 .:  $IE \approx IC$ 

Here UBE = 0.7V for & & VBE = 0.2V for Gre

- -> By selecting a proper value of RE, we can obtain a desired
  - value of emitter current for a known value of VEE.
- -> The emitter cutyent in transistors Q1 & Q2 is independent of collector resistance RC.

### to determine VCEQ:

Assume mat the voltage drop across Rin is negligibly small. Then the voltage at the emitter of transistor Q1 is approximately equal to -NBE.

-) voltage at collector Vc = Vcc-IcRc

collector-to-emitter voltage VCE = VC - VE

VIE = VIC-TICEC - (- VIBE)

VCE = VCC + VBE - ICRC

Note: The dc analysis equations (1) + (2) are applicable too all four DA consigurations as long as we use the same biasing arrangement for each of them.

- -> To perform ac analysis to derive the expression for the voltage gain Ad, elp resistance Ri & olp resistance Ro of the DA.
  - 1. Set the dc voltages +VCC & -VEE at Zero
  - 2. Substitute the Small-Signal T-equivalent models for the toansistoss.

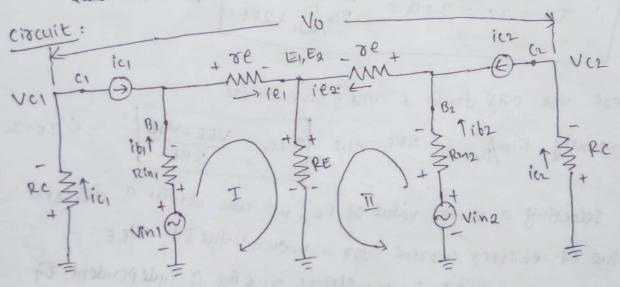
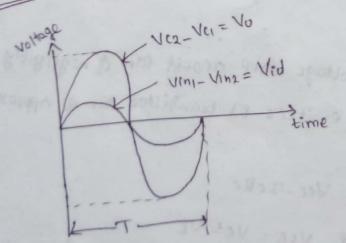


fig (c). Ac equallalent circuit of Dual ilp, Balance of DA



vinj- Vinz = Vid figld): | p 4 olp wave formy

Voltage Gain (Ad):

Note: \* IEI=IE2; re1=re2=re

\* 1/p & olp are out of phase by 180°.

\* The voltage at collector ca is assumed to be more positive with respect to collector ci, even though both of them wie negative wish respect to ground.

Generally Rinz/Pac value is very Small hence neglected

→ Equations (1) & (2) can be solved Simultaneously for ie 1 & ie2 by using Cramer's rule:

$$|e| = \frac{|V_{in1}| |RE|}{|V_{in2}| |V_{in2}| |RE|} = \frac{(\sigma_e + RE) |V_{in1}| - (RE) |V_{in2}|}{(\sigma_e + RE)^2 - (RE)^2}$$

The o/p voltage 
$$Vo = Vc_2 - Vc_1$$

$$Vo = -Rc_2ic_2 - (-Rc_1ic_1)$$

$$Vo = Rc_1ic_1 - Rc_1ic_2$$

$$Vo = Rc_2ic_1 - Rc_1ic_2$$

$$Vo = Rc_2ic_1 - Rc_2ic_2$$

Substitute current relations ie 1 & iez in above equation.

Vo = Rc 
$$\left[\frac{(\text{Ye+Re}) \text{Vin}_1 - (\text{Re}) \text{Vin}_2}{(\text{Ye+Re})^2 - (\text{Re})^2} - \frac{(\text{Ye+Re}) \text{Vin}_2 - (\text{Re}) \text{Vin}_2}{(\text{Ye+Re})^2 - (\text{Re})^2}\right]$$

Vo = Rc  $\left[\frac{(\text{Ye+Re}) (\text{Vin}_1 - \text{Vin}_2) + (\text{Re}) (\text{Vin}_1 - \text{Vin}_2)}{(\text{Ye+Re})^2 - (\text{Re})^2}\right]$ 

Vo = Rc  $\left[\frac{(\text{Vin}_1 - \text{Vin}_2) (\text{Ye+Re+Re})}{\text{Ye} + \text{Ye} + \text{Re}} - \text{Ye}}\right]$ 

Vo = Rc  $\left[\frac{(\text{Vin}_1 - \text{Vin}_2) (\text{Ye+Re})}{\text{Ye} + \text{Ye}}\right]$ 
 $\left[\frac{(\text{Yo} + \text{Re})^2 - (\text{Re})^2}{(\text{Ye})^2}\right]$ 
 $\left[\frac{(\text{Yo} + \text{Re})^2 - (\text{Re})^2}{(\text{Ye})^2}\right]$ 
 $\left[\frac{(\text{Ye+Re}) \text{Vin}_1 - \text{Vin}_2}{(\text{Ye+Re})^2}\right]$ 
 $\left[\frac{(\text{Ye+Re}) \text{Vin}_1 - \text{Vin}_2}{(\text{Ye+Re})^2}\right]$ 

E2(3) represents DA amplifies the difference blu two ilp Signals.

Sig(c): Shows the ilp& olp waveforms of dual ilp, balanced olp DA.

By defining Vid = Vin1-Vin2 as the difference in ilp voltages.

E2(4) represents voltage gain of differential Amplifier (DA). which is independent of RE.

-> Differential E/P resistance is defined as the equivalent resistance that would be measured at either Elp terminal with the other terminal grounded.

\* The i/p resistance Ril is seen from the i/p Signal source Vin1 is determined with the Signal source vin2 set at Zero.

\* Similarly the ilp resistance Riz is seen from the ilp signal source Vinz is determined with the signal source vin 1 set at zero.

-> usually the Source resistances Rin1 & Rin2 are very Small and hence will be ignored in the devivation of ilp resistances Rij & Riz.

$$Ril = \frac{|Vin 1|}{|ib|} |Vin 2 = 0$$

$$Ril = \frac{|Vin 1|}{|ie|} |Vin 2 = 0$$

$$\therefore ibl = \frac{|e|}{|ae|} |Pac|$$

Substitute the value of ier in the above equation

$$Ril = \frac{\beta ac \ Vinl}{(\forall e+RE) \ Vinl - (RE)(0)}$$

$$Ril = \frac{\beta ac \ Vinl}{(\forall e+RE) \ Vinl} \frac{(\forall e+RE) \ Vinl}{(\forall e+RE) \ Re+RE = RE}$$

$$Ril = \frac{\beta ac \ \forall e \ (2RE)}{RE}$$

$$Ril = \frac{\beta ac \ \forall e \ (2RE)}{RE}$$

$$Ril = \frac{\beta ac \ \forall e \ (2RE)}{RE}$$

Similarly Ri2 = 
$$\left| \frac{Vin2}{ib2} \right| Vin_{1}=0$$
  
Ri2 =  $\left| \frac{Vin2}{ie2/\beta_{ac}} \right| Vin_{1}=0$ 

Substitute les value in the above equation.

$$Ri2 = \frac{Vin2 \, \beta ac}{(\text{Ye+RE}) \, \text{Vin2} - (\text{RE})(o)} = \frac{Vin2 \, \beta ac}{(\text{Ye+RE})^2 - (\text{RE})^2}$$

$$Ri2 = \frac{\beta ac}{(\text{Ye} + \text{RE})}$$

#### Out put Registance ;

It is defined as the equivalent resistance that would be measured at either of terminals with respect to ground.

- -> The off resistance Roi measured blu collector Ci & ground is equal to that of the collector resistor Rc.
- -) Similarly the off resistance RO2 measured at collector c2 with respect to ground is equal to that of the collector resistor RC.

\* The current gain of differential amplifier (DA) is undefined therefore it will not be derived for any of the four configurations.

\* There fore DA is generally used as a voltage amplifier and not as a current (81) Power amplifier.

In this configuration two P/P Signals are used; now ever, the ofp is measured at only one of the two collectors with respect to ground. Hence the olp is an unbalanced olp.

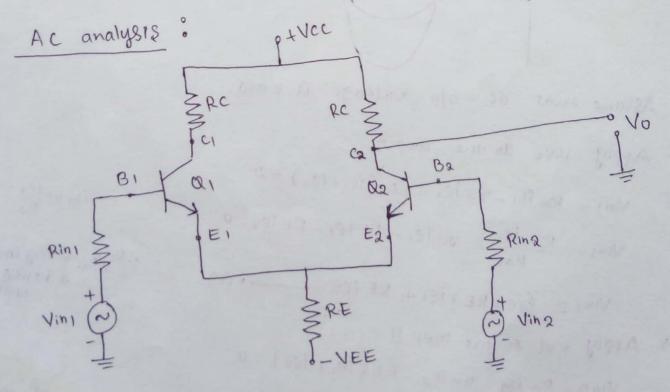
Let us assume that the olp is measured at the collector of transistor Q2 with respect to ground. See fig: 2(a)

### . DC analysis:

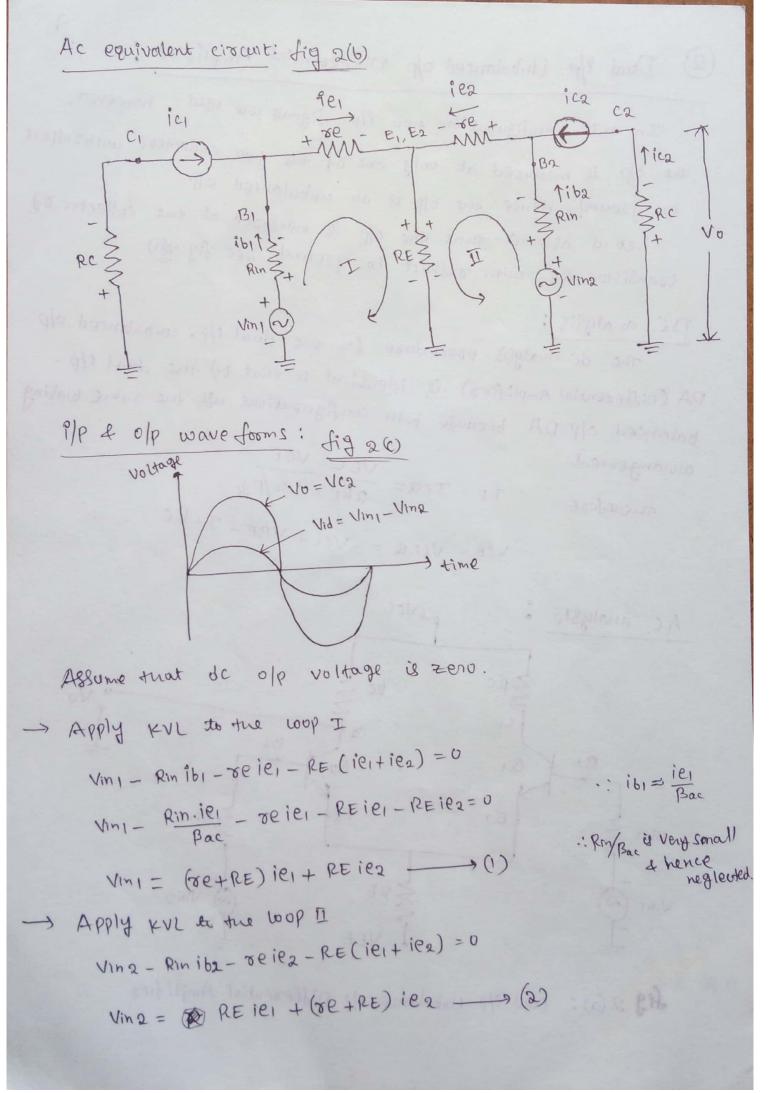
The dc analysis procedure for the dual i/p, unbalanced o/p DA (Differential Amplifiers) is identical to that of the dual i/p. balanced of DA because both configurations use the same biasing arrangement.

IE = ICR = VEE - VBE

2RE+ Rin/Bdc Therefore VCE = VCEQ = VCC + VBE - ICRC



Lig 2(a): Dual i/P. unbalance of Differential Amplifier



## Differential i/p Resistance:

The only difference blw dualip, balanced of PDA & dual i/p unbalanced olp DA is in the way of olp voltage measured. However, the 1/P resistance seen from either ilp sources does not depend on the way of op voltage measured. Therefore, the ilp resistance Ri Seen from either ilp source of the dual i/p, unbalanced of DA should be same as that of the dual ilp, balanced olp DA is given by equations

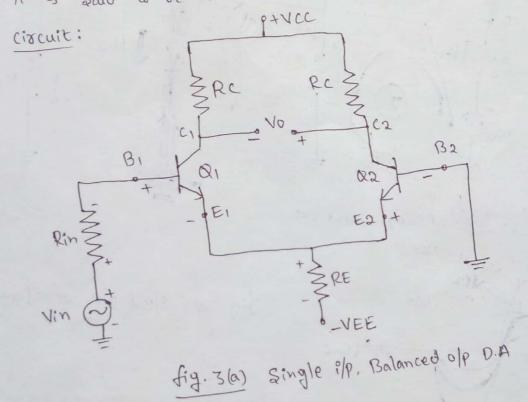
Ril = Ri2 = 2 Bacre

## Out put resistance

the olp resistance Ro measured at collector ca with respect to ground is equal to the collector resistor RC. Thus Ro = RC

# 3). Single P/P, Balanced o/P Differential Ampliffer:

In this configuration the single P/P signal is applied to base of transistor Q1, and the off is measured blu the two collectors, which are at the same dc potential. Therefore, the off is Said to be a balanced off.



### DC analysis:

The dc analysis procedure for the Single Pp, balanced ofp differential amplifier (D.A) is identical to that of the previous two differential amplifier configurations. Because all configurations use the same biosing avangement

There fore

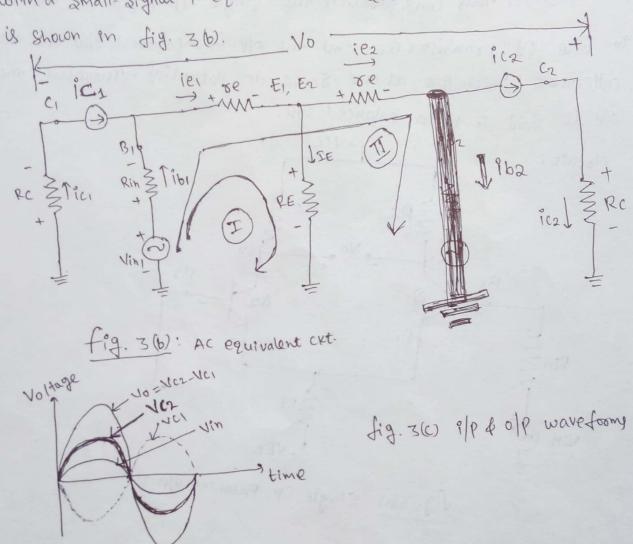
IE = ICQ = VEE - VBE

REP - VBE

VCE = VCC + VBE - ICRC

#### AC analysis:

The ac equivalent circuit of the Single ilp, balance olp DA with a Small-Signal T-equivalent model Substituted for the transistor



- During the Positive half cycle of P/P Signal, the base-emitter voltage of a is positive & that of a is negative, as shown in fig. 3(a) This means that the collector current on a increases & that in a decreases from the operating point value Ica. Hence the current of both sources icitics are shown to be in the Same direction
- During the negative half cycle of i/p Signal, the opposit action takes place. i.e., the collector current of transistor Q1 decreases and that in transistor Q2 encreases.

- The polarity of voltage across each collector resistor is consistent with the direction of current sources ic & ica.

  That is voltage across collector resistor of the ig positive and that across the collector of the ignerative with respect to the ground.
- -> According to this polovity, the off voltage is equal to the voltage at collector C1.

### Voltage Cruin (Ad) ?

-> Apply KUL for LOOP I & II OF fig. 3(6)

Vin - Rinibi - reiei - RE(iei-ie2) =0

Vin- Rmibi - reili - reilez zo

-> Substitute current relations ib= ie1 Bac & ib2 = ie2 Bac

Vin - Rin iei - Veiei - REiei + REiez=0

Vin - Rin iei - reiei - reiez=0

-) Generally, Rin/Bac value is very Small; there for for simplicity we shall neglect it and rearrange the equations as follows.

Counting (1) & (2) can be solved simultaneously fore ie, & iea by using coanser's rule. (retre) vin

Substitute the ilik ilz values in the above equations.

then 
$$V_0 = RC \left[ \frac{(RE) Vin}{re[re+2RE]} + \frac{(re+RE) Vin}{re[re+2RE]} \right]$$

Note: The Voltuge gain of Single-ilp, balanced of DA is equal to trust of the dual 1/p, balanced of DA

i/p resistance:

It is seen from the PP Signal Source is determed as fallows.

·: Ri = 2 Bacre

Op Resistance:

- -) It is me equivalent resistance that would be measured at either off terminal with respect to ground.
- -> merefore, the old resistance Rol measured at the collector Cif the old resistance Ros measured at the collector co are given by

In this configuration the P/P signal is applied to the base of transistor Q1, and the o/P is measured at the collector of transistor Q2.

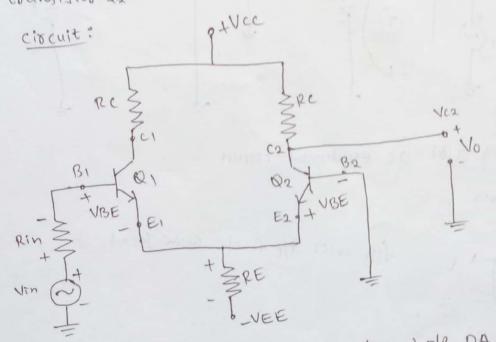


fig. 4(a) single i/p, unbalanced olp. DA;

### DC analysis:

The dc analysis procedure for the single P/P, unbalanced ofp differential amplifier is identical to that of the previous three differential amplifier configurations. Because all configurations use the same biosing arrangement.

There fore,

$$TE = TCQ = \frac{VEE - VBE}{2RE + RIN/Bdc}$$
 $VCE = VCEQ = VCC + VBE - TCCC$ 

### AC analysis:

The ac equivalent circuit of single ilp, unbalanced olp disferential amplifier with a small-signal 7-equivalent model substituted for the toansistor is shown in fig. 4(b).

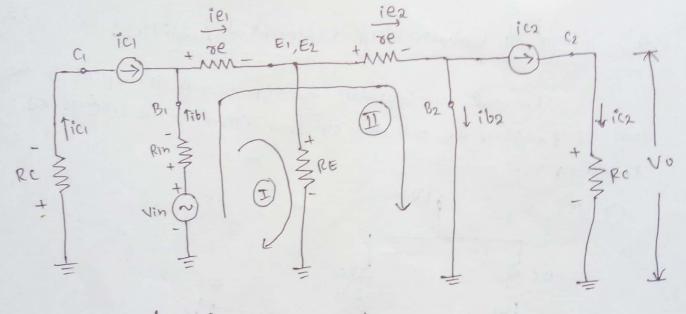


fig. 4(b) ac equivalent circuit

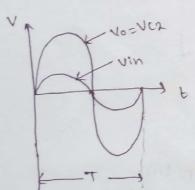


fig. 4(c) i/p & o/p wave forms.

Voltage gain:

-> apply KVL to the loop I & I

Vin-Rinibi- reiei-RE(iei-iea) =0

vin - Rinibi - reiel - reien = 0

-> Substitute current relations i'b1 = ie1 & ib2 = ie2 Bac

Vin- Riniel - veiel - REiel + REiel =0

Vin - Riniel - ve iel - ve ie2=0

-> Generally. Rin/Bac value is very small; therefore for simplicity we shall neglect this value & recovering the equations as follows

equations (D& (2) can be solved Simultaneously for i'e, & i'e,

The o/p voltage is  $V_0 = V_{C2} = RC i_{C2} = RC i_{C2}$   $V_0 = RC \frac{V_{in}(RE)}{ve[ve+2RE)}$   $V_0 = RC \frac{V_{in}(RE)}{ve[ve+2RE)} = \frac{RC V_{in}}{2ve}$   $V_0 = \frac{RC}{2ve} = Ad$   $V_0 = \frac{RC}{2ve} = Ad$   $V_0 = \frac{RC}{2ve} = Ad$ 

Note: the voltage gain of Single ilp, unbalanced olp differential amplifier is is half the gain of Single ilp balanced olp differential amplifier.

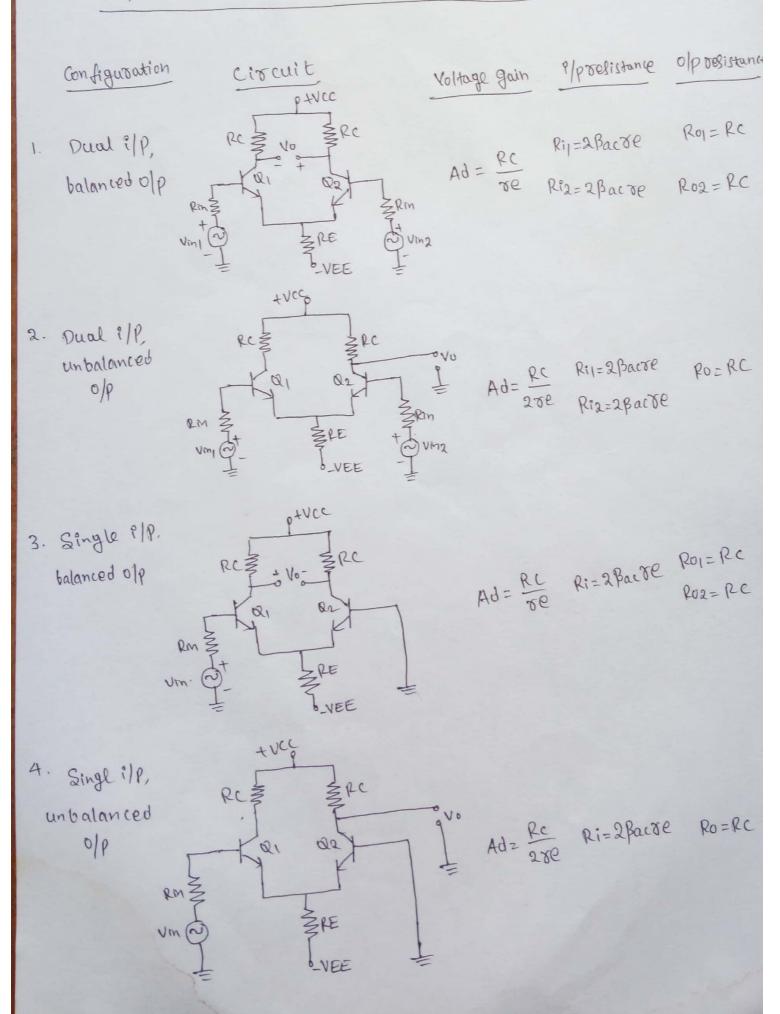
It is seen from the ip Signal Source is determined

8677 RE

VETARE = 2RE

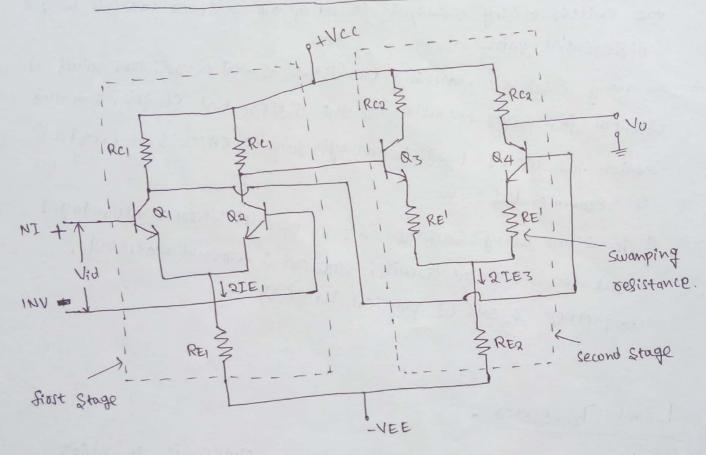
### ofp Resistance:

to ground is equal to the collector resistor RC.



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# Cascaded Differential Amplifier Stages:



- The two Stuge differential amplifier can be coscaded in Series is shown in above figure.
- The first Stage is a dual-i/p, balanced-olp differential amplifier the Second Stage is a dual-i/p, unbalanced-olp differential amplifier, driven by the first D.A.
- The first stage used an emitter resistance REI, which couries a current 2TEI, where TEI is emitter current of QI. which is same as emitter current of Q2 as the transistors are perfectly matched.
- The Second Stage used a point of swamping resistances and an emitter resistance REQ. This couries a current 2 TEZ, where TEZ is emitter current to 03 which same as emitter current to 04 as the two transistors are perfectly matched.

- -) A Single-ended of is taken from this second Stage. Both Stages use the emitter biosing technique to set-up the emitter currents in the differential points.
- In many cases the matching transistors as well as resistors values is essential for proper operation of the differential stages. For this reason the use of transistor arrays such as CA 3086 @ LM 3146 is recommended
  - -> A transistor array Such as CA 3086 provides inherent advantages unique to integrated circuits: electrical & theornal matching, compactness & ease of physical handing

### Level Translator:

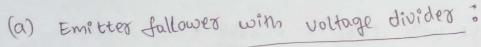
The main purpose of Level translator is to shift the ofp de level towards the ground, with minimum change in the ac Signal

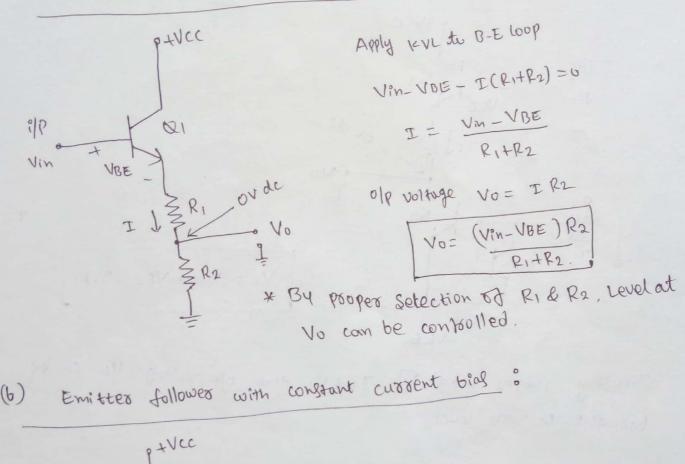
Because of the direct coupling, the dc level at emitter risely from Stuge to Stage. This increase dc level tends to Shift the operating point of the succeeding Stuges and therefore limits the oppositions swing and may even distort the ofp Signal.

Therefore in the cascaded differential amplifies, to shift the off dc level down to zero volts, the second (on) final Stage must be fallowed by a level translator circuit.

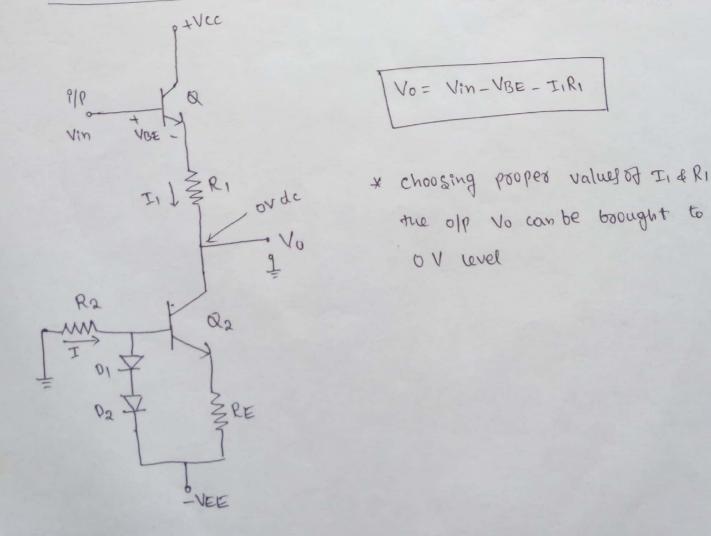
a) Emitter fallower with voltage divider

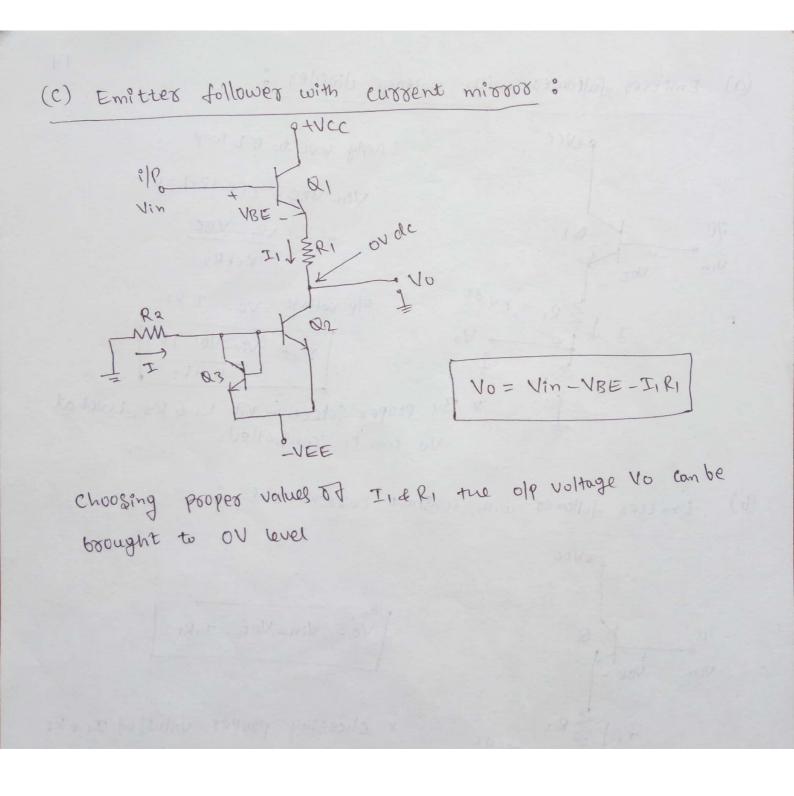
- b) " " constant current bias
- c) 11 11 current mirror





# (b) Emitter follower with constant current bias:







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#### IC Features and Difference b/w AIC & DIC

- 1. Input Offset Voltage.
- 2. Input Offset Current.
- 3. Input Bias Current.
- 4. Differential Input Resistance.
- 5. Input Capacitance.
- 6. Input Voltage Range.
- 7. Common Mode Rejection Ratio (CMRR).
- 8. Supply Voltage Rejection Ratio (SVRR).



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L.B.Reddy Nagar, Mylavaram-521230, Krishna Dist, Andhra Pradesh, India



### **Specifications of Differential Amplifiers**

- 1. High differential voltage gain
- 2. Low common mode gain
- 3. High CMRR
- 4. High input resistance
- 5. Low output resistance
- 6. Low offset voltage
- 7. Low offset current
- 8. Large bandwidth
- 9. Two input terminals

